



# VHDL for Logic Synthesis

*Andrew Rushton*

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VHDL for Logic Synthesis Second Edition Andrew Rushton TransEDA Limited, Southampton, UK Very high-speed integrated circuit Hardware Description Language (VHDL) is the worldwide standard for computer-aided electronic system design. Logic synthesis automates gate-level design, allowing the designer to concentrate on a register-transfer level implementation. VHDL for Logic Synthesis provides comprehensive coverage of the language and its role in the generation of hardware. This enhanced second edition takes a broader view of the use of synthesis and its place in the design cycle. Features include: Explanation of each aspect of the language in hardware terms and demonstration of the mapping from VHDL to hardware Updated examples using the standard packages numeric\_std and std\_logic\_1164 plus more illustrative models offering further source references for designers Additional chapter on std\_logic\_arith to aid designers still working with this popular package New focus on libraries and library management covering the contents of the standard library, how to use library work and recommendations on code management Extra section detailing how to use assertions to report diagnostics, allowing the reader to print signal and variable values to the screen Senior undergraduate and postgraduate students of microelectronics and digital hardware engineers new to language-based design methods will appreciate Rushton's informative introduction to VHDL and its use in logic synthesis.

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